High Frequency Receiver

BACKGROUND OF THE INVENTION

5   1. Field of the Invention

The present invention relates to a high frequency receiver for receiving a broadband high frequency signal.

2. Background Art

10   A conventional tuner will be described hereinafter with reference to a drawing.   Fig. 26 is a schematic block diagram of the conventional tuner.

In Fig. 26, a high frequency signal of about 50 to 860 MHz is fed into input terminal 1.

Antenna filter 2 connected to input terminal 1 is a single tuning filter.

15   Tuned frequency by antenna filter 2 is tuned to a frequency of a received channel, and an undesired frequency is removed.   High-frequency amplifier 3 is connected to an output part of antenna filter 2 and amplifies the high frequency signal.

An output part of high frequency amplifier 3 is connected to step-to-step

20   filter 4.   Step-to-step filter 4 is a double tuning filter.

Mixer 5 is a double balanced mixer, and one input part thereof is connected to the output part of step-to-step filter 4 and the other input part is connected to the output part of frequency-variable local oscillator 6.   Mixer 5 converts the frequency of a signal to a predetermined intermediate frequency

25   (IF).

Band-pass filter 7 receives an output from mixer 5, and removes signals other than a desired signal.   An output from band-pass filter 7 is supplied to

output terminal 8.

Japanese Patent Examined Publication No. H7-297682, for example, is known as prior art information related to the present invention.

The frequency conversion by a mixer generally generates an image

5   interfering signal, so that an image (this is simply called an image) for generating the image interfering signal must be previously suppressed with a filter on the upstream side of the mixer. The conventional high frequency receiver therefore increases a damping amount of the image with respect to frequency, using a filter having a high-performance damping characteristic in a

10   two-stage structure of a single tuning filter and a double tuning filter.

The conventional high frequency receiver requires two filters, namely one double tuning filter having two tuning circuits and one single tuning filter, so that the receiver is expensive.

15   SUMMARY OF THE INVENTION

The present invention provides a high frequency receiver having the following elements:

an input terminal for receiving a high frequency signal;

a filter connected to the input terminal;

20   a mixer of which one input part is connected to an output part of the filter and the other input part is connected to an output part of a frequency-variable local oscillator; and

an output terminal connected to an output part of the mixer.

The mixer is an image rejection mixer. The filter has a moderated damping

25   characteristic at a frequency where the image rejection mixer reduces the image.

                          BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram of a high frequency receiver in accordance with exemplary embodiment 1 of the present invention.

Fig. 2 is a schematic diagram showing a relation of frequencies and signals in accordance with exemplary embodiment 1.

5 Fig. 3A, Fig. 3B, Fig. 3C and Fig. 3D show respective phase relations between desired signals and image interfering signals in accordance with exemplary embodiment 1.

Fig. 4 is a damping characteristic diagram of a filter in accordance with exemplary embodiment 1.

10 Fig. 5 is another damping characteristic diagram of the filter in accordance with exemplary embodiment 1.

Fig. 6 illustrates an image by triple harmonic wave in accordance with exemplary embodiment 1.

Fig. 7 is a block diagram of a high frequency receiver in accordance with 15 exemplary embodiment 2 of the present invention.

Fig. 8A and Fig. 8B are characteristic diagrams of a filter and a phase shifter in accordance with exemplary embodiment 2.

Fig. 9 is a block diagram of a high frequency receiver in accordance with exemplary embodiment 3 of the present invention.

20 Fig. 10 is a characteristic diagram of a low-pass filter in accordance with exemplary embodiment 3.

Fig. 11 is a block diagram of a high frequency receiver in accordance with exemplary embodiment 4 of the present invention.

Fig. 12 is a block diagram of a high frequency receiver in accordance with 25 exemplary embodiment 5 of the present invention.

Fig. 13 is a block diagram of a high frequency receiver in accordance with exemplary embodiment 6 of the present invention.

Fig. 14 is a circuit diagram of an input filter in accordance with exemplary embodiment 7 of the present invention.

Fig. 15A and Fig. 15B are equivalent circuit diagrams in accordance with exemplary embodiment 7.

Fig. 16A and Fig. 16B are impedance characteristic diagrams in accordance with exemplary embodiment 7.

Fig. 17A and Fig. 17B are damping characteristic diagrams in accordance with exemplary embodiment 7.

Fig. 18 is another circuit diagram of an input filter in accordance with exemplary embodiment 8 of the present invention.

Fig. 19A and Fig. 19B are equivalent circuit diagrams in accordance with exemplary embodiment 8.

Fig. 20A and Fig. 20B are impedance characteristic diagrams in accordance with exemplary embodiment 8.

Fig. 21A and Fig. 21B are damping characteristic diagrams in accordance with exemplary embodiment 8.

Fig. 22 is a sectional view of a high frequency receiver in accordance with exemplary embodiment 9 of the present invention.

Fig. 23 is a top view of the high frequency receiver in accordance with exemplary embodiment 9.

Fig. 24 is an expanded view of a shield case of the high frequency receiver in accordance with exemplary embodiment 9.

Fig. 25A and Fig. 25B are detail drawings of essential parts of the high frequency receiver in accordance with exemplary embodiment 9.

Fig. 26 is a block diagram of a conventional high frequency receiver.

DETAILED DESCRIPTION OF THE INVENTION

(Exemplary embodiment 1)

Exemplary embodiment 1 of the present invention will be hereinafter described with reference to the drawings. Fig. 1 is a block diagram of a high frequency receiver in accordance with exemplary embodiment 1.

5   In Fig. 1, input terminal 20 receives a high frequency signal of a television broadcast of about 50 to 860 MHz.

Input filter 21 is connected to input terminal 20. In Exemplary embodiment 1, input filter 21 is formed of a circuit having only one set of tuning circuits where an inductance and a variable capacitance diode are connected in

10   parallel. This circuit is hereinafter called a single tuning circuit. Tuned frequency of input filter 21 is varied by changing voltage applied to the variable capacitance diode. When the high frequency receiver receives a desired channel, voltage is applied to the variable capacitance diode so that the tuned frequency of input filter 21 substantially equals to the frequency of the desired channel.

15   Signals other than the signal in the desired channel can thus be damped.

High frequency amplifier 22 is connected to an output part of input filter 21, and amplifies high frequency signals having passed through input filter 21. High frequency amplifier 22 is a variable gain amplifier capable of varying gain with a control voltage applied to control terminal 22a.

20   High frequency amplifier 22 is thus disposed, so that the high frequency receiver can have high noise figure (NF) in a system even when a device having low NF is used downstream. Since input filter 21 is disposed upstream of high frequency amplifier 22, undesired signals inputted into high frequency amplifier 22 can be removed.

25   It is important that an input level of signals fed into high frequency amplifier 22 is set at a level for preventing saturation of high frequency amplifier 22. Signals with a high level causing the saturation of high frequency amplifier

22 distort, and undesired signals such as higher harmonic waves occur in high frequency amplifier 22. Therefore, it is important that signals other than the desired signal are damped to a level where high frequency amplifier 22 does not saturate. Since input filter 21 is a single tuning circuit, damping characteristics

5   of both upside frequency and downside frequency of the tuned frequency are obtained.

Fixed filter 23 is a second filter connected to the output part of high frequency amplifier 22. Second filter 23 has a natural cutoff frequency determined based on a fixed inductance and a fixed capacitance. Second filter

10   23 is a low-pass filter and has a cutoff frequency of about 349 MHz in embodiment 1.

The output part of the second filter is connected to unbalanced/balanced converter 24, and converts an unbalanced circuit to a balanced circuit. When all circuits are essentially formed of balanced circuits and connected in a balanced

15   state, immunity against interruption or the like of an interfering signal from the outside can be improved. For balancing input filter 21 and second filter 23, two sets of the filters are required for each of the filters. However, the circuits keep balance hardly and become expensive when a discrete configuration is employed, so that a part after second filter 23 is converted to a balanced circuit.

20   The output part of unbalanced/balanced converter 24 is connected to image rejection mixer (IRM) 25, and is formed of a balanced circuit. IRM 25 is formed of two sets of double balanced mixers (DBMs) 26, 27 and two sets of phase shifters 28, 29. The mixer is formed of the balanced circuit, so that a distortion characteristic of the mixer can be improved and interference hardly

25   occurs in the mixer.

In IRM 25, the output part of unbalanced/balanced converter 24 is firstly divided into two. One output part of unbalanced/balanced converter 24 is

connected to one input part of DBM 26, and an output part of frequency-variable local oscillator 30 is connected to the other input part of DBM 26. The output part of DBM 26 is connected to phase shifter 28.

The other output part of unbalanced/balanced converter 24 is connected to
5   one input part of DBM 27, and the other input part of DBM 27 is connected to another output part of frequency-variable local oscillator 30 via phase shifter 29. An output of DBM 27 and an output of phase shifter 28 are combined.

Phase shifter 28 and phase shifter 29 change phases of signals inputted into these phase shifters by 90°. Phase shifter 29 delays the phase of an
10   oscillation frequency signal of frequency-variable local oscillator 30 by 90° so that the phase of a signal having an intermediate frequency as the output of DBM 27 delays by 90°. Phase shifter 28 delays the phase of a signal having an intermediate frequency supplied from DBM 26 by 90°.

IRM 25 having such a configuration mixes an output signal of frequency-
15   variable local oscillator 30 and a signal of a desired channel, and frequency-converts the signal of the desired channel to an intermediate frequency signal having 45.75 MHz. Frequency-variable local oscillator 30 of embodiment 1 is of the upper heterodyne type where oscillation frequency of oscillator 30 is higher than the frequency of the desired channel signal by the frequency (this is
20   hereinafter called intermediate frequency) of the intermediate frequency signal.

Balanced/unbalanced converter 31 is disposed so as to receive a combined signal of an output of phase shifter 28 and an output of DBM 27. Balanced/unbalanced converter 31 converts the circuit to the unbalanced circuit. The output part of the balanced/unbalanced converter 31 is connected to
25   intermediate frequency filter 32. In embodiment 1, the center of the passing band of intermediate frequency filter 32 is substantially intermediate frequency, and filter 32 damps a signal having a frequency separated from the intermediate

frequency by 3 MHz or higher. The frequency of 3 MHz is a half of the frequency band of 6MHz of substantially one channel.

Intermediate frequency filter 32 is unbalanced, so that balanced/unbalanced converter 31 is disposed before filter 32. The output part of filter 32 is connected to output terminal 33. Intermediate frequency filter 32 may be balanced for improving the distortion characteristic, and in this case balanced/unbalanced converter 31 is operated as a buffer circuit. Phase locked loop (PLL) circuit 34 is loop-connected to frequency-variable local oscillator 30.

Since the oscillation frequency of oscillator 30 depends on the frequency of the desired channel signal in embodiment 1, phase shifter 29 must have enough accuracy to stably shift the phase in a wide frequency band. Phase shifter 29 is a so-called flip-flop type phase shifter. This shifter includes frequency doubler 35 for multiplying the signal of frequency-variable local oscillator 30, and frequency divider 36 connected to the output part of frequency doubler 35. Frequency divider 36 returns the output frequency of frequency doubler 35 to the original oscillation frequency. At this time, the phase of an input signal to DBM 27 can be shifted by 90°.

While, phase shifter 28 is simply required to shift the phase only of intermediate frequency. Therefore, a polyphase type phase shifter having a high phase change accuracy of the frequency at a certain point is employed to shift the phase of the output signal of DBM 26 by 90°.

Next, a mechanism for generating image interference and an operation for suppressing the image interference with the IRM used in the high frequency receiver of embodiment 1 are described with reference to the drawings. Fig. 2 is a schematic diagram showing a relation between frequencies and signals. Fig. 3A, Fig. 3B, Fig. 3C and Fig. 3D show respective relations between desired signals and image interfering signals in the IRM of exemplary embodiment 1.

In Fig. 2, horizontal axis 40 shows frequency and vertical axis 41 shows level. An example where the second channel of a television broadcast in the United States of America is described. Frequency 43 of signal 42 of the desired channel is about 55.25 MHz. Oscillation frequency 45 of oscillation signal 44 of frequency-variable local oscillator 30 is frequency difference 48 higher than frequency 43 of the signal of the desired channel. In this case, frequency 46 of intermediate frequency signal 47 is 45.75 MHz, so that frequency of oscillation frequency 45 is 101 MHz. A mixer mixes oscillation signal 44 having oscillation frequency 45 and desired channel signal 42 having frequency 43, and outputs a signal having intermediate frequency 46 equal to frequency difference 48 between oscillation signal 44 and desired channel signal 42.

Occurrence of image interfering signal 49 is then described. Image interfering signal 49 occurs when an unnecessary signal exists in signals fed into the mixer. Here, for example, the unnecessary signal is a signal that is mixed with the signal of frequency-variable local oscillator 30 and converted into the same frequency as that of intermediate frequency signal 47 by the mixer. In other words, the mixer outputs a frequency difference between two inputted frequencies, so that a signal having frequency image 50 higher than oscillation frequency 45 by frequency difference 48 is converted into the intermediate frequency. Here, frequency difference 48 is a difference between desired channel signal 42 and the signal of oscillator 30.

A signal that is converted by the mixer and generates image interfering signal 49 having the frequency same as intermediate frequency 46 is called image 51, frequency 52 of image 51 in embodiment 1 is 146.75 MHz.

Image 51 is generated in three cases:

a broadcast signal itself existing on or near frequency 52 becomes image 51;

image 51 is generated from a plurality of broadcast signals 54, 55 that have a frequency higher than frequency 52 of image 51 and between which frequency difference 53 equals to frequency 52 of image 51; and inversely,

image 51 is generated from a plurality of broadcast signals 56, 57 that

5   have a frequency lower than frequency 52 of image 51 and of which frequencies are summed into a value equal to frequency 52 of image 51.

Additionally, a case where sum of or difference between frequencies of three or more broadcast signals equals to frequency 52 of image 51 is also considered. These image interferences cause problems in a high frequency receiver.   The

10   high frequency receiver is, for example, an electronic tuner for receiving the television broadcast that converts a desired channel signal into intermediate frequency 46 lower than oscillation frequency 45 and has a wide received frequency band.

Next, an operation of the IRM of embodiment 1 for suppressing image 51

15   generated by the mixer is hereinafter described with reference to the drawings. Fig. 3A, Fig. 3B, Fig. 3C and Fig. 3D show respective phase relations of desired signals and image interfering signals in the IRM of embodiment 1.

Fig. 3A shows phases of output signals supplied from DBM 26.   DBM 26 simply converts frequency, and hence desired channel signal 60 and image

20   interfering signal 61 have the same phase.

Fig. 3B shows phases of intermediate frequency signal 66 and image interfering signal 67 in the output signals of phase shifter 28.   Phase shifter 28 delays phases of the outputs of DBM 26 by 90° and delays both phases of intermediate frequency signal 66 and image interfering signal 67 by 90°.

25   Fig. 3C shows phases of output signals supplied from DBM 27.   When DBM 27 mixes a signal of which phase is delayed by 90° by phase shifter 29 and the desired channel signal, phase 63 of intermediate frequency signal 62

outputted from DBM 27 is delayed by 90°.

Image 50 mixed with oscillation frequency 45 by DBM 27 inverses frequency relation between the desired channel signal and the oscillation signal, so that the phase of image interfering signal 64 in the output of DBM 27 shifts in
5   the direction opposite to intermediate frequency signal 62. Phase 65 of image interfering signal 64 is advanced by 90°.

Fig. 3D shows a combined state of the output signals of DBM 27 and the output signals of phase shifter 28. The combined signals are supplied to balanced/unbalanced converter 31. Intermediate frequency signals 62, 66 thus
10   have the same phase. The phase difference between image interfering signal 64 and image interfering signal 67 is 180° in the output of IRM 25, so that the image interfering signals cancel each other out. Therefore, logically, the image interfering signals can be completely removed. In other words, IRM 25 can not only convert frequency as a double balanced mixer but also cancel an image.
15   Signals having the image suppressed discussed above are supplied to balanced/unbalanced converter 31.

However, realistically, it is difficult to keep the accuracy with which two phase shifters change the phase of the image interfering signal by just 180°. That is because the phase change disperses for frequencies of the phase shifters,
20   or the phase change disperses every phase shifter, for example. In this case, difference between the phases of the image interfering signals is not just 180°, so that the image interfering signals cannot be completely cancelled out each other and cannot be entirely removed.

Additionally, distortion or the like of DBM 26 or DBM 27 causes a
25   harmonic signal, and the harmonic signal generates an image interfering signal. IRM 25 of embodiment 1 can suppress the image interfering signal by about 30 dB.

The high frequency receiver of the present invention moderates a damping amount of the filter by a suppressed amount of the image interfering signal by IRM 25, at the frequency of the image for generating the image interfering signal or the frequency for generating an image by combining a plurality of signals.

5   Next, a relation between IRM 25 and a damping characteristic of the filter is described.   Fig. 4 and Fig. 5 show damping characteristic diagrams of the filter in accordance with exemplary embodiment 1.   The horizontal axis shows frequency, and the vertical axis shows signal level of the filter or damping amount.

10   In Fig. 4, a case where the desired channel is set at the VHF2 channel, for example, is described.   Frequency 70 of the VHF2 channel in North America is about 55.25 MHz.   Intermediate frequency 71 in North America is 45.25 MHz, so that frequency 73 of image 72 suppressed by IRM 25 is 146.75 MHz.

For providing image interfering signal 74 with a level 75 at which   signal 74 does not affect a picture or the like, level 76 of image 72 must be suppressed by about 60 dB.   IRM 25 can suppress the level of image 72 by about 30 dB, so that image interference does not occur even when the damping amount of image 72 by the filter at frequency 73 (146.75 MHz) is reduced to about 30 dB.

For suppressing the image interfering signal, a sharp damping characteristic such as damping characteristic 77 is required when the employed mixer is a normal DBM.   When the employed mixer is an IRM, however, a filter can be used which has a moderated damping amount of about 30 dB at frequency 73 and has a gentle damping characteristic such as damping characteristic 78.

Fig. 5 shows suppression of the image generated by a plurality of high frequency signals in embodiment 1.   In Fig. 5, an ultra high frequency (UHF) channel is assumed, and elements similar to those in Fig. 4 are denoted with the same reference numbers and the descriptions of those elements are omitted.

Frequency 70a of the UHF channel in North America is about 505.25 MHz.

Image 72a is generated from the sum of two frequencies 80 (295.25 MHz) and 81 (301.25 MHz) lower than frequency 70a of the desired channel. The IRM

5   inverts the phase of image 72a itself to cancel out image 72a itself. An image generated by a plurality of high frequency signals can be also suppressed, so that the damping characteristics of the filter at frequencies 80, 81 can be moderated.

Thanks to the configuration discussed above, a filter having a large damping amount, a sharp damping characteristic, and high performance is not

10   required. Even a filter having a gentle damping characteristic can prevent the image interference. In other words, when the IRM is employed in the high frequency receiver having a wide receiving band, the damping amount can be reduced at a specific frequency for generating the image interfering signal. Therefore, an inexpensive filter can be employed, and an inexpensive high

15   frequency receiver can be provided.

Since the mixer of embodiment 1 is IRM 25, the damping amount of image 51 at frequency 52 can be kept to be about 30 dB and image 51 can be suppressed by 60 dB when input filter 21 is a single tuning circuit. Even only one tuning circuit can prevent the image interference, so that the filter can be inexpensive

20   and an inexpensive high frequency receiver can be realized.

Second filter 23 is a fixed filter in embodiment 1, so that only one tuning circuit is employed and the tuned frequency need not be adjusted. Therefore, a high frequency receiver having high productivity can be provided.

Since only input filter 21 has the tuning circuit, Q value of the tuning

25   circuit less changes with respect to the frequency and shift of the matching of the impedance is reduced. Variation of gain and waveform every channel is therefore reduced, so that stable receiving can be realized. This is important

especially when a digital broadcast is received, and this configuration allows realization of an inexpensive digital receiving tuner.

Additionally, the high frequency receiver of embodiment 1 employs a low-pass filter having cutoff frequency of about 349 MHz as second filter 23. When the receiver receives low frequency signals capable of passing through the low-pass filter, the image occurrence due to a signal having high frequency of 349 MHz or higher can be suppressed.

According to an operation analysis, the IRM cannot remove an image interfering signal that is generated by an interference occurring at a frequency higher by the intermediate frequency than triple harmonic wave of oscillation frequency 45 of frequency-variable local oscillator 30. This interference is hereinafter called a third harmonic image. In embodiment 1, second filter 23 is the low-pass filter, and the image generated by the third harmonic of oscillator 30 when the channel having lowest frequency is received is made to have the cutoff frequency. The third harmonic image is therefore prevented from causing interference.

This preventing operation is described specifically with reference to the drawing. Fig. 6 shows an image caused by the triple harmonic wave. An example of receiving the VHF2 channel, namely the channel having the lowest frequency, is described with reference to Fig. 6. When the VHF2 channel is received, oscillation frequency 45 of frequency-variable local oscillator 30 is 101 MHz. Frequency 92 of third harmonic image 91 corresponding to third harmonic 90 of oscillator 30 is about 349 MHz, namely higher than frequency 93 of third harmonic 90 by intermediate frequency 46. The interference is caused by third harmonic image 91 in IRM 25, so that interference by the third harmonic image is prevented by previously removing third harmonic image 91 itself with filter 21 or 23 on the upstream side of IRM 25.

Spuriouses by broadcast signals having a frequency of 349 MHz or higher can be suppressed, so that mutual interference by the spuriouses can be simultaneously prevented.

Second filter 23 damps the signal of third harmonic image 91 in
5   embodiment 1; however, a filter for damping third harmonic image 91 may be disposed before input filter 21 and input terminal 20.   In the latter case, third harmonic image 91 or undesired signal is prevented from being fed into high frequency amplifier 22, so that distortion of amplifier 22 can be reduced.

When a lower frequency such as the frequency in the VHF channel of the
10   electronic tuner is received, for example, the cutoff frequency of the low-pass filter is set at about 360 MHz near a high end of the substantially VHF channel. Thus, image occurrence caused by the spurious or the like by a plurality of broadcast signals in the UHF band can be suppressed, and hence the image interference can be prevented.   Here, the UHF band is not lower than the cutoff
15   frequency.

A low-pass filter is used as the fixed filter in embodiment 1; however, a band-pass filter may be used.   In the latter case, in receiving frequency capable of passing through the band-pass filter, the following image interferences can be prevented:

20   an image interference caused by a signal having a high frequency not lower than the cutoff frequency on the upside of the band-pass filter; and

an image interference caused by a signal having a low frequency not higher than the cutoff frequency on the downside of the band-pass filter.

A high-pass filter may be used as the fixed filter.   In this case, when a
25   higher frequency such as the frequency in the UHF channel of the electronic tuner is received, for example, the cutoff frequency of the high-pass filter is set to be in the UHF band.   Thus, image occurrence caused by the spurious or the like

by a plurality of broadcast signals in the VHF band can be suppressed, and hence the image interference can be prevented. Here, the VHF band is not higher than the cutoff frequency.

5   A plurality of filters having a different pass band may be disposed and switched in response to a desired channel. A filter for reducing image occurrence can be thus selected in response to the desired channel. Therefore, a signal for generating an image interfering signal can be therefore suppressed over wider frequency.

IRM 25 is formed of a balanced circuit in embodiment 1, so that immunity
10   against interruption or the like of an interfering signal can be improved, a stable mixer can be realized, and respective circuits can be disposed adjacently. A small high frequency receiver can be therefore obtained.

The damping amount of image 51 at frequency 52 is required simply to be secured at about 30 dB, so that input filter 21 may be formed of a double tuning
15   circuit, for example, and high frequency amplifier 22 may be directly connected to unbalanced/balanced converter 24. Otherwise, unbalanced/balanced converter 24 may be interposed between high frequency amplifier 22 and input filter 21, high frequency amplifier 22 may be formed of a balanced circuit, and high frequency amplifier 22 may be directly connected to IRM 25. Signal loss
20   can be reduced between high frequency amplifier 22 and IRM 25 in both configurations, so that degradation of the NF between them can be prevented. Therefore, even when a transistor having low NF is used in high frequency amplifier 22, the NF of the entire system can be kept.

Since the transistor having low NF is used in high frequency amplifier 22,
25   an inexpensive transistor such as a bipolar transistor can be used and an inexpensive high frequency receiver can be realized. IRM 25, frequency-variable local oscillator 30, and PLL 34 are integrated circuits using a bipolar

transistor, so that high frequency amplifier 22, IRM 25, frequency-variable local oscillator 30, and PLL 34 can be stored in one integrated circuit, and a small high frequency receiver can be realized.

Second filter 23 is a fixed filter, but it may be a single tuning filter or a
5   double tuning filter.   Second filter 23 can therefore, further improve the damping characteristic at the frequency for generating an image interfering signal.   Occurrence of image interference can be further prevented.

Input filter 21 is a single tuning filter in embodiment 1; however, input filter 21 may be a fixed filter especially in a small television capable of
10   permitting an interference characteristic.   In the latter case, filter loss is reduced, so that NF is improved and the filter is effective for the electronic tuner for a small television of which receiving sensitivity characteristic is important.

Phase shifter 28 of embodiment 1 is formed of a poly-phase type filer including a capacitor and a resistor, so that phase shifter 28 does not require
15   electric power.   The high frequency receiver therefore requires less electric power, so that the receiver is extremely useful for portable equipment such as a cellular phone.

In the high frequency receiver of embodiment 1, a step-to-step filter is a fixed filter and interposed between the high frequency amplifier and the image
20   rejection mixer.   This configuration allows prevention of the image interference even when there are less tuning circuits.   A tuning circuit is disposed only in the input filter, so that the Q value of the tuning circuit less changes with respect to the frequency and the shift of the matching of the impedance is reduced. Variation of gain and waveform every channel is therefore reduced, so that
25   stable receiving can be realized.   This is important especially when a digital broadcast is received, and this configuration allows realization of an inexpensive digital receiving tuner.

(Exemplary embodiment 2)

Exemplary embodiment 2 of the present invention will be hereinafter described with reference to the drawings. Fig. 7 is a block diagram of a high frequency receiver in accordance with exemplary embodiment 2. In Fig. 7, elements similar to those in Fig. 1 are denoted with the same reference numbers and the descriptions of those elements are omitted.

In Fig. 7, frequency-variable local oscillator 30 is formed of three oscillators. Frequency-variable local oscillator 30 is generally formed of a circuit including a variable capacitance diode and an inductor element. One oscillator cannot completely cover the entire oscillation frequency region of frequency-variable local oscillator 30, so that a plurality of oscillators are generally employed. In embodiment 2, the entire oscillation frequency region is divided into three frequency bands, and oscillators 100, 101, and 102 cover respective frequency bands. Switch 104 is interposed between power supply terminal 103 and oscillators 100, 101, and 102, and selectively connects power supply terminal 103 to one of oscillators 100, 101, and 102. An input filter of embodiment 2 is formed of a single tuning circuit.

Fig. 8A shows an image damping amount by the filter with respect to received frequency in embodiment 2, and Fig. 8B shows a relation between the received frequency and a phase shift amount by phase shifters 28, 29.

In Fig. 8A and Fig. 8B, horizontal axis 110 shows the received frequency. Vertical axis 111 of Fig. 8A shows the sum of image damping amounts by input filter 21 and second filter 23. Vertical axis 112 of Fig. 8B shows a phase shift amount by the phase shifters.

In Fig. 8A and Fig. 8B, first frequency band 113 is a VHF low band and the frequency in this band ranges from 55.25 MHz to 127.25 MHz. Second

frequency band 114 is a VHF high band, and the frequency in this band ranges from 133.25 MHz to 343.25 MHz. Third frequency band 115 is a UHF band, and the frequency in this band ranges from 349.25 MHz to 801.25 MHz.

5   According to the relation between the damping amount by the filter and the frequency, the damping amount depends on the frequency. The tuning circuit constituting input filter 21 employs a parallel resonant circuit, so that load Q is apt to decrease to degrade a damping characteristic at a higher frequency in the band. The higher frequency of the UHF band has no problem because the image frequency is higher than the receiving band. However, in

10   the VHF band, especially in the VHF low band hardly forming an image trap, the degradation of the damping characteristic at the higher frequency raises a problem.

According to the relation between the received frequency and a phase shift amount by phase shifters 28, 29, phase shift curve 119 of phase shifter 29 shows

15   that the phase shift amount of phase shifter 29 is apt to change every band. Phase shift curve 120 of phase shifter 28 shows that phase shifter 28 keeps the phase substantially constant independently of the frequency of a received channel. Phase shifter 28 is simply required to change the phase only of the intermediate frequency regardless of the desired channel, so that a poly-phase

20   type phase shifter or the like may be used and a phase shifter having high phase shift accuracy can be provided.

In embodiment 2, phase shift 119 of phase shifter 29 with respect to first frequency band 113 where the damping amount by the filter is minimum is set closest to 90°, and the image suppressing amount in IRM 25 is increased.

25   A channel having a small damping amount by filter 21 is matched with a channel having a large image damping amount in IRM 25, thereby compensating a shortfall of the damping amount by the filter and suppressing an

image in a wide receiving frequency band.

(Exemplary embodiment 3)

Exemplary embodiment 3 of the present invention will be hereinafter

5   described with reference to the drawings. Fig. 9 is a block diagram of a high
frequency receiver in accordance with exemplary embodiment 3. In Fig. 9,
elements similar to those in Fig. 1 are denoted with the same reference numbers
and the descriptions of those elements are omitted.

In Fig. 9, switch 130 has common terminal 130a connected to the output

10   part of high frequency amplifier 22, and three output terminals 130b, 130c, and
130d. Switch 130 selectively switches among output terminals 130b, 130c, and
130d. First output terminal 130b is directly connected to IRM 25. First low-
pass filter 131 is interposed between second output terminal 130c and IRM 25.
Second low-pass filter 132 is interposed between the output part of third output

15   terminal 130d and IRM 25.

Channel-select-data generator 135 has one output part connected to PLL
34, and generates channel select data based on desired channel information
inputted to input terminal 135a of channel select data generator 135. PLL 34
determines frequency of frequency-variable local oscillator 30 based on the

20   channel select data. Controller 136 is interposed between the other output part
of channel select data generator 135 and switch 130, and switches to an
appropriate output terminal in response to channel select data generator 135.

As shown in Fig. 10, cutoff frequency 137 of low-pass filter 131 is 133.25
MHz, and cutoff frequency 138 of low-pass filter 132 is 349.25 MHz, for example.

25   For receiving a VHF low band in this case, controller 136 selects output terminal
130b. For receiving a VHF high band, controller 136 selects output terminal
130c. For receiving a UHF band in this case, controller 136 selects output

terminal 130d. An undesired signal can be thus prevented from being fed into IRM 25, so that image interference can be suppressed. In the UHF band, image frequency itself often lies out of a receiving band, so that only the damping characteristic of input filter 21 is required and signals are fed into IRM 25

5   directly without passing through the filter.

The low-pass filter is employed in embodiment 3; however, a band-pass filter, a high-pass filter, or a combination of them may be employed in response to a received frequency band or existence of a signal for generating an image.

10   (Exemplary embodiment 4)

Exemplary embodiment 4 of the present invention will be hereinafter described with reference to the drawings. Fig. 11 is a block diagram of a high frequency receiver in accordance with exemplary embodiment 4. In Fig. 11, elements similar to those in Fig. 1 are denoted with the same reference numbers

15   and the descriptions of those elements are omitted.

In embodiment 4, two high frequency receivers according to embodiment 1 are connected in parallel, high-pass filter 140 is interposed between input terminal 20 and input filter 21a of one high frequency amplifier 22a, and low-pass filter 141 is interposed between input terminal 20 and input filter 21b of the

20   other high frequency amplifier 22b. Cutoff frequencies of high-pass filter 140 and low-pass filter 141 are about 350 MHz, namely frequency of a low-end channel of a substantially UHF band in embodiment 4.

The VHF channel is received by receiving unit 142 on the side having low-pass filter 141, and the UHF channel is received by receiving unit 143 on the side

25   having high-pass filter 140. The separate receiving units therefore receive the VHF and UHF. In receiving the UHF, a frequency that is IF frequency lower or higher than higher harmonic wave lies out of the receiving band. Here, the

higher harmonic wave has a frequency more than three times the oscillation frequency of local oscillator 30. No filter is therefore required between high frequency amplifier 22a and IRM 25a. Therefore, loss can be decreased between high frequency amplifier 22a and IRM 25a, so that the NF of the entire

5　system can be improved.

While, the lowest frequency of triple harmonic wave image occurring in the VHF channel is provided when the channel having the lowest frequency is received. Therefore, when second filter 24b is interposed so that a frequency not lower than the lowest frequency of the triple harmonic wave image is the cutoff

10　frequency, the image interference characteristic can be improved.

(Exemplary embodiment 5)

Exemplary embodiment 5 of the present invention will be hereinafter described with reference to the drawings. Fig. 12 is a block diagram of a digital

15　tuner for receiving ground wave in accordance with exemplary embodiment 5. In Fig. 12, elements similar to those in Fig. 1 are denoted with the same reference numbers and the descriptions of those elements are omitted.

In Fig. 12, switch 150 is interposed between high frequency amplifier 22 and IRM 25. Switch 150 has common terminal 150a connected to the output

20　part of high frequency amplifier 22, and has output terminals 150b, 150c. Output terminal 150b is connected to IRM 25. DBM 151 is interposed between output terminal 150c and output terminal 33.

Both output parts of IRM 25 and DBM 151 are connected to demodulator 152. Error corrector 153 is disposed between the output part of demodulator

25　152 and output terminal 33. Error corrector 153 is formed of Viterbi corrector 154 and reed solomon corrector 155 connected to one output part of Viterbi corrector 154. The other output part of Viterbi corrector 154 is connected to

determining device 156, and controller 157 is disposed between the output part of determining device 156 and switch control terminal 150d of switch 150.

Determining device 156 determines a bit error rate of an output of Viterbi corrector 154. When determining device 156 determines that the bit error rate

5   is a predetermined value or higher, determining device 156 outputs a signal for commanding the controller to connect switch 150 to the IRM 25 side.

When the image interference has degraded the bit error rate, the IRM can prevent the image interference and hence the bit error rate can be improved. When no image signal exists and the bit error rate is high, the DBM can be used

10   and hence power consumption can be reduced.

When the bit error rate of an output of Viterbi corrector 154 is generally 0.0002 or lower, reed solomon corrector 155 corrects the output to change the bit error rate at output terminal 33 to zero. When the bit error rate becomes 0.0002 or higher, determining device 156 transmits, to controller 157, a signal

15   indicating that the bit error rate exceeds 0.0002. On receiving the signal, controller 157 transmits a signal for commanding switch 150 to switch between mixers.

When the bit error rate does not increase even if the mixer is switched from DBM 151 to IRM 25, determining device 156 determines that the fact that

20   the bit error rate exceeds 0.0002 is not caused by an image, and returns the mixer to the DBM.

(Exemplary embodiment 6)

Exemplary embodiment 6 of the present invention will be hereinafter

25   described with reference to the drawings. Fig. 13 is a block diagram of a digital tuner for receiving ground wave in accordance with exemplary embodiment 6. In Fig. 13, elements similar to those in Fig. 1 and Fig. 12 are denoted with the

same reference numbers and the descriptions of those elements are omitted.

In Fig. 13, switch 160 is interposed between the output part of high frequency amplifier 22 and DBM 27. Controller 161 is interposed between ON/OFF control terminal 160a of switch 160 and determining device 156.

5   Switch 162 is disposed so as to control power supply to phase shifter 29. Switch 162 is connected so that controller 161 can control ON or OFF.

Controller 161 outputs a signal for turning on switches 160, 162 when the bit error rate exceeds 0.0002. In other words, when switches 160, 162 are usually turned off, high frequency signals are supplied only to the DBM 26 side,

10   phase shifter 29 and DBM 27 do not operate, and hence the power consumption can be reduced. When the bit error rate increases, controller 161 functions as the IRM by turning on switches 160, 162, thereby preventing an image.

Phase shifter 28 employs a poly-phase filter in embodiment 6; however, phase shifter 28 may be a phase shifter of a flip-flop type by multi-ply and

15   division similarly to phase shifter 29.

(Exemplary embodiment 7)

Exemplary embodiment 7 of the present invention will be hereinafter described with reference to the drawings. Fig. 14 is a circuit diagram of an

20   input filter in accordance with exemplary embodiment 7 of the present invention.

In embodiment 7, a variable image trap is disposed in the input filter. In Fig. 14, the input filter is interposed between input terminal 160 and output terminal 163. Input terminal 160 is connected to a series connection body of first inductance 161 and second inductance 162. Output terminal 163 is

25   connected to one of output parts of second inductance 162, and variable capacitance diode 164 is interposed between the other of the output parts and the ground. The anode side of variable capacitance diode 164 is grounded.

Input terminal 160 is connected to a series connection body of third inductance 165 and switch 166 in parallel with first inductance 161. Switch 166 is turned off in receiving a VHF low band, or turned on in receiving a VHF high band.

5 Fourth inductance 167 is interposed between the output part of third inductance 165 and the ground. For changing capacitance of variable capacitance diode 164, control voltage supplied to control terminal 168 connected to the cathode side of variable capacitance diode 164 is varied.

In tuning filter 169 having this configuration, second variable capacitance 10 diode 170 is interposed between fourth inductance 167 and the ground, and control terminal 168 is connected to the cathode-side terminal of second variable capacitance diode 170 to form a variable trap.

Constants of respective circuits of embodiment 7 are as follows: first inductance 161 is 300 nH, second inductance 162 is 70 nH, third inductance 165 15 is 40 nH, and fourth inductance 167 is 40 nH. While, capacitances of variable capacitance diodes 164, 170 are changed from 60 pF to 3 pF by changing control voltage from 1V to 25V.

Operations of the input filter are described with reference to Fig. 15A, Fig. 15B, Fig. 16A, Fig. 16B, Fig. 17A, and Fig. 17B. Fig. 15A and Fig. 15B are 20 equivalent circuit diagrams of the input filter in accordance with exemplary embodiment 7. Fig. 16A and Fig. 16B are impedance characteristic diagrams of the input filter. Fig. 17A and Fig. 17B are damping characteristic diagrams of the input filter.

An operation performed when the input filter of embodiment 7 receives a 25 VHF low band is described. Fig. 15A shows an equivalent circuit used when the input filter of embodiment 7 receives the VHF low band. Switch 166 is turned off in this case, so that first inductance 161 and second inductance 162 form first

equivalent inductance 180, and third inductance 165 and fourth inductance 167 form second equivalent inductance 181. First equivalent inductance 180 corresponds to 80 nH, and second equivalent inductance 181 corresponds to 370 nH.

5   The input filter is therefore formed of a parallel resonance circuit and a trap circuit of a series resonance circuit. The parallel resonance circuit has first equivalent inductance 180, second equivalent inductance 181, and the capacitance of first variable capacitance diode 164. The series resonance circuit has second equivalent inductance 181 and the capacitance of second variable

10   capacitance diode 170.

Fig. 16A shows impedance provided when the input filter of embodiment 7 receives the VHF low band. Horizontal axis 190 shows frequency, and vertical axis 191 shows impedance. Fig. 17A shows a damping characteristic provided when the input filter receives the VHF low band. Horizontal axis 210 shows

15   frequency, and vertical axis 211 shows damping amount.

In Fig. 16A, curve 192 shows variation of impedance with respect to the frequency of the input filter. The impedance of the input filter varies from C-component to L-component as the frequency exceeds a parallel resonance frequency for tuning in response to the capacitance of variable capacitance diode

20   170. Pole 194 occurs due to the series resonance at specific frequency 193 higher than the tuned frequency. The impedance is zero at pole 194, so that the damping characteristic of the input filter increases at frequency 193 as shown in Fig. 17A.

Constants of second equivalent inductance 181 and the capacitance of

25   variable capacitance diode 170 are determined so that frequency 193 of pole 194 equals to the frequency of the image of a received channel in embodiment 7. Trap frequency 210a is changed in response to the received channel by changing

the capacitance of variable capacitance diode 170, as shown in Fig. 17A.

Curve 195 shows impedance provided when no variable capacitance diode 170 exists and fourth inductance 167 is directly grounded in Fig. 16A. As shown in Fig. 16A, variation of the impedance is small near the parallel

5 resonance frequency for tuning of the input filter regardless of the existence of variable capacitance diode 170. In other words, the variation of the impedance increases in response to the capacitance of variable capacitance diode 170 in the direction where the frequency is higher than the parallel resonance frequency for tuning. Therefore, the impedance near the resonance frequency does not

10 largely vary even when the capacitance of variable capacitance diode 170 is varied.

An operation performed when the input filter of embodiment 7 receives a VHF high band is described. Fig. 15B shows an equivalent circuit used when the input filter of embodiment 7 receives the VHF high band. Switch 166 is

15 turned on in this case. First inductance 161 is 300 nH and third inductance 165 is 40 nH, so that the impedance on the third inductance 165 side is dominant and first inductance 161 may be neglected in embodiment 7.

The input filter is therefore formed of a parallel resonance circuit and a trap circuit of a series resonance circuit. The parallel resonance circuit includes

20 second inductance 162, fourth inductance 167, and the capacitance of first variable capacitance diode 164. The series resonance circuit has fourth inductance 167 and the capacitance of second variable capacitance diode 170.

Fig. 16B shows impedance provided when the input filter of embodiment 7 receives the VHF high band. Horizontal axis 200 shows frequency, and vertical

25 axis 201 shows impedance. Fig. 17B shows a damping characteristic provided when the input filter receives the VHF high band. Horizontal axis 220 shows frequency, and vertical axis 221 shows damping amount.

In Fig. 16B, curve 202 shows variation of impedance with respect to the frequency of the input filter. The impedance of the input filter varies from L-component to C-component as the frequency becomes lower than a parallel resonance frequency for tuning in response to the capacitance of variable

5 capacitance diode 170. Pole 204 occurs due to the series resonance at specific frequency 203 lower than the tuned frequency. The impedance is zero at pole 204, so that the damping characteristic of the input filter increases at frequency 203 as shown in Fig. 17B.

Frequency 203 of pole 204 works as a trap of the frequency band of the

10 VHF low band, and trap frequency 222 is varied by changing the capacitance of variable capacitance diode 170 in embodiment 7, as shown in Fig. 17B.

Curve 205 shows impedance provided when no capacitance of variable capacitance diode 170 exists and fourth inductance 167 is directly grounded in Fig. 16B. As shown in Fig. 16B, variation of the impedance is small near the

15 resonance frequency of the input filter regardless of the existence of variable capacitance diode 170. In other words, the variation of the impedance increases in response to the capacitance of variable capacitance diode 170 in the direction where the frequency is lower than the parallel resonance frequency for tuning. Therefore, the impedance near the parallel resonance frequency for tuning does

20 not largely vary even when the capacitance of variable capacitance diode 170 is varied.

(Exemplary embodiment 8)

Exemplary embodiment 8 of the present invention will be hereinafter

25 described with reference to the drawings. Fig. 18 is a circuit diagram of an input filter in accordance with exemplary embodiment 8. A fixed image trap is disposed in the input filter.

In Fig. 18, the input filter is interposed between input terminal 250 and output terminal 255. Input terminal 250 is connected to first inductance 251, second inductance 252, and third inductance 254 in series.

One of output parts of third inductance 254 is connected to output terminal 255, and variable capacitance diode 256 is interposed between the other of the output parts of third inductance 254 and the ground. The anode side of variable capacitance diode 256 is grounded.

A series connection body of fourth inductance 257 and switch 258 is interposed between input terminal 250 and third inductance 254, and fifth inductance 259 is interposed between the output part of fourth inductance 257 and the ground. Switch 258 is turned off in receiving a VHF low band, or turned on in receiving a VHF high band.

Changing the capacitance of variable capacitance diode 256 varies the tuned frequency of the tuning circuit. In other words, control voltage supplied to control terminal 260 connected to the cathode side of variable capacitance diode 256 is varied in response to a received channel. Capacitor 253 is disposed in parallel with second inductance 252 to form a fixed trap.

Constants of respective circuits of embodiment 8 are as follows: first inductance 251 is 300 nH, second inductance 252 is 60 nH, third inductance 254 is 70 nH, fourth inductance 257 is 40 nH, and fifth inductance 259 is 40 nH. While, capacitance of variable capacitance diodes 256 is varied from 60 pF to 3 pF by changing control voltage from 1V to 25V.

Operations of the input filter are described with reference to Fig. 19A, Fig. 19B, Fig. 20A, Fig. 20B, Fig. 21A, and Fig. 21B. Fig. 19A and Fig. 19B are equivalent circuit diagrams of the input filter in accordance with exemplary embodiment 8. Fig. 20A and Fig. 20B are impedance characteristic diagrams of the input filter. Fig. 21A and Fig. 21B are damping characteristic diagrams of

the input filter.

An operation performed when the input filter of embodiment 8 receives a VHF low band is described. Fig. 19A shows an equivalent circuit used when the input filter of embodiment 8 receives the VHF low band. Switch 258 is turned off in this case, so that first inductance 251 and third inductance 254 form first equivalent inductance 270, and fourth inductance 257 and fifth inductance 259 form second equivalent inductance 271. First equivalent inductance 270 corresponds to 370 nH, and second equivalent inductance 271 corresponds to 80 nH.

The input filter is therefore formed of a parallel resonance circuit and a fixed trap circuit. The parallel resonance circuit has first equivalent inductance 270, second equivalent inductance 271, the capacitance of variable capacitance diode 256, and second inductance 252. The fixed trap circuit has second inductance 252 and capacitor 253.

Fig. 20A shows impedance provided when the input filter of embodiment 8 receives the VHF low band. Horizontal axis 280 shows frequency, and vertical axis 281 shows impedance. Fig. 21A shows a damping characteristic provided when the input filter receives the VHF low band. Horizontal axis 300 shows frequency, and vertical axis 301 shows damping amount.

In Fig. 20A, curve 282 shows variation of impedance with respect to the frequency of the input filter. The impedance of the input filter varies from C-component to L-component as the frequency exceeds a parallel resonance frequency for tuning in response to the capacitance of capacitor 253. Pole 284 occurs at specific frequency 283 higher than the tuned frequency. The impedance is zero at pole 284, so that the damping characteristic of the input filter increases at frequency 283 as shown in Fig. 21A.

Each constant is determined in embodiment 8 so that frequency 283 of

pole 284 equals to the frequency of the image for a substantially central channel of the VHF low band.

However, the image frequency in receiving the VHF low band lies within the frequency band of the VHF high band. Trap frequency 283 of the fixed trap of embodiment 8 lies within the frequency band of the VHF high band. Therefore, when the trap operates also in receiving the VHF high band, a signal in the channel near trap frequency 283 is damped by the fixed trap and hence can be received.

Therefore, when the VHF high band is received in the input filter of embodiment 8, switch 258 is turned on to prevent an operation of the trap circuit having second inductance 252 and capacitor 253.

An operation performed when the input filter of embodiment 8 receives a VHF high band is described. Fig. 19B shows an equivalent circuit used when the input filter of embodiment 8 receives the VHF high band. In embodiment 8, first inductance 251 is 300 nH and fourth inductance 257 is 40 nH, so that the impedance on the fourth inductance 257 side is dominant. In this case, first inductance 251, second inductance 252, and capacitor 253 may be neglected.

The input filter has only a parallel resonance circuit having fifth inductance 259, fourth inductance 257, third inductance 254, and the capacitance of variable capacitance diode 256. In this case, a trap circuit does not work, so that no pole occurs in receiving the VHF high band as shown in Fig. 20B. As shown in Fig. 21B, therefore, there is no trap for damping a specific frequency and the fixed trap hardly produces an effect in receiving the VHF high band.

(Exemplary embodiment 9)

Exemplary embodiment 9 of the present invention will be hereinafter

described with reference to the drawings. In exemplary embodiment 9, a high frequency receiver of the present invention is stored in a shield case. Fig. 22 is a sectional view of the high frequency receiver in accordance with exemplary embodiment 9. Fig. 23 is a top view of the high frequency receiver. Fig. 24 is

5   an expanded view of the shield case of the high frequency receiver of exemplary embodiment 9. Fig. 25A and Fig. 25B are detail drawings of essential parts of the high frequency receiver of exemplary embodiment 9.

In Fig. 22 to Fig. 25A and Fig. 25B, electronic component 401 is mounted on one surface 400a of printed board 400 and connected to printed board 400

10   with cream solder 402. Inductances 403 are mounted on the other surface 400b of printed board 400. Each inductance 403 is a coil, and legs 403a thereof are inserted into holes formed in printed board 400. Legs 403a are joined to printed board 400 with solder 402.

Shield case 404 is engaged with printed board 400 on which electronic

15   component 401 and inductance 403 are previously mounted to form a high frequency circuit. The ground part of the high frequency circuit is soldered and connected to frame 404a of shield case 404 at the peripheral edge of printed board 400.

Shield case 404 has lid 404b for covering the side having inductance 403,

20   and lid 404b is formed integrally with frame 400a of printed board 400. Lid 404b has legs 404c formed by cutting and bending a part of lid 404b. The tips of legs 404c penetrate printed board 400, and are joined to printed board 400 with solder 402 on the mounted side of electronic component 401.

Cover 405 for covering the opening of shield case 404 is mounted to the

25   mounted side of electronic component 401. Cover 405 includes elastic contact claw 406 or abutting part 407. Elastic contact claw 406 or abutting part 407 is butted on the tip of each leg 404c to act as a shield.

In embodiment 9, width 408 of each leg 404c is substantially equal to width 409 of each inductance 403, and inductance 403 is disposed closely to leg 404c. Especially, a ground part of a circuit formed of coil 403a is connected to the leg disposed closely to coil 403a.

5   Leg 404c is especially and preferably disposed in the magnetic flux direction of inductance 403, as shown in Fig. 25B. When an air-core coil is used as inductance 403, for example, it is important that opening surface 410 of coil 403a faces wide surface 411 of leg 404c.

In this configuration, magnetic flux 412 generated by inductance 403 can

10   be shielded by leg 404c, thereby preventing coupling with the other inductance.

The damping characteristic of the filter of the high-frequency receiver can be moderated using the IRM, discussed in embodiment 1. The number of tuning filters apt to couple to each other especially due to the magnetic flux can be therefore decreased. The high-frequency receiver of the present invention

15   having the configuration of embodiment 9 requires only a small number of easy-to-couple coils 403a for the tuning filter, so that even a simple shield prevents the coupling with the other coil.

Frame 404a, lid 404b, and legs 404c are integrally formed in shield case 404 of embodiment 9, so that the ground can be kept stably for vibration or the

20   like. An interval between coil 403a and the lid does not vary, so that the inductance value becomes stable to decrease waveform variation of the filter.

Frame 404a, lid 404b, and legs 404c can be simultaneously machined by press working or the like, so that an inexpensive shield case can be obtained and an inexpensive high-frequency receiver can be realized. The cover exists only

25   on one side, so that assembling is facilitated and assembling man-hour can be reduced.

Coil 403a is disposed outside a bending part of leg 404c. In this case, coil

403a is disposed under hole 413 produced by cutting and bending the leg 404c. Hole 413 can be used also as a hole for adjustment. While, coil 403b is disposed inside a bending part of the other leg 404c. No hole exists over coil 403b, so that the magnetic flux of coil 403b can be further shielded to prevent coupling to the

5   other coil, interruption of an undesired signal from the outside, and leakage of a signal.

The air-core coil is used as the inductance in embodiment 9; however, a chip inductor or a pattern coil may by used. In the latter case, the coupling to the other inductance can also be reduced.

10   Q value of the chip inductor or the pattern coil is generally smaller than that of the air-core coil, and is easily affected by a neighboring metal plate or the like. In embodiment 9, however, width 408 of leg 404c is substantially equal to width 409 of the inductance, so that leg 404c is prevented from reducing the Q value of the pattern inductance or the chip inductance. This prevention is

15   important for keeping selectivity and reducing loss of the tuning filter when the tuning filter is formed using the inductance. Thus, in the configuration of embodiment 9, a good filter can be obtained even when the pattern inductance or the chip inductance is used as the inductance.

The high frequency receiver of the present invention has the following

20   elements:

an input terminal for receiving a high frequency signal;

a filter connected to the input terminal;

a mixer of which one input part is connected to an output part of the filter and the other input part is connected to an output part of a frequency-

25   variable local oscillator; and

an output terminal connected to an output part of the mixer.

The mixer is an image rejection mixer. The filter has a moderated damping

characteristic in frequency where the image rejection mixer reduces the image.

Since the image rejection mixer reduces the image, a damping amount of the image with respect to the frequency may be reduced in the filter. A high-performance filter is not required, so that the inexpensive high frequency receiver can be advantageously provided.

The high frequency receiver of the single conversion type of the upper heterodyne type for receiving a signal having a broadband frequency is interfered by many signals existing in the receiving band. Therefore, image interference generated by a combination of the many signals must be suppressed. In the high frequency receiver of the present invention, an image suppressing characteristic by an IRM and a damping characteristic by a filter suppress the image in response to the received frequency and prevent the image interference. The damping characteristic is used for damping an image itself or a signal for generating the image.

The damping amount by the filter may be small, so that a complex configuration having three tuning circuits is not required differently from a conventional filter, the filter can be replaced by a fixed filter or the like, and the number of tuning circuits can be decreased. The number of components constituting the filter can be therefore reduced, so that an inexpensive and small high frequency receiver can be provided.

When tuning circuits are used, Q values of the tuning circuits and a matching property between them vary with respect to the frequency. However, the number of tuning circuits can be decreased in the present invention, so that this variation can be reduced. Variation of the gain or waveform every channel can be therefore reduced, and the reduction is useful especially when signals of a digital television broadcast are received.

Reducing the tuning circuits can decrease the number of adjusting places

and time for adjusting the high frequency receiver, so that productivity is extremely improved and an inexpensive high frequency receiver can be provided.

Reducing the tuning circuits can decrease coupling between coils constituting the tuning circuits, so that the shied of the shield case can be

5   simplified and an inexpensive high frequency receiver can be realized.